PCB Layout and Design Guide for CH7108B HDMI To SDTV Converter

1.0 INTRODUCTION

The CH7108B is a low-cost, low-power semiconductor device, which can convert HDMI signals into SDTV outputs with IIS or SPDIF audio output.

This application note focuses only on the basic PCB layout and design guidelines for CH7108B Converter. Guidelines in component placement, power supply decoupling, grounding, input /output signal interface are discussed in this document. The discussion and figures that follow reflect and describe connections based on the 40-pin QFN package of the CH7108B. Please refer to the CH7108B datasheet for the details of the pin assignments.

2.0 COMPONENT PLACEMENT AND DESIGN CONSIDERATIONS

Components associated with the CH7108B should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C1, C2, C4, C6, C7, C9, C10, C12) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7108B ground pins, in addition to ground vias.

2.1.1 Ground Pins

The grounds of the CH7108B should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7108B ground pins should be connected to its respective decoupling capacitor ground lead directly, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

The power supply includes VDDPLL, DVDD, AVCC, AVCC_DAC, and AVDD. Refer to **Table 1** for the Power supply pins assignment. Refer to **Figure 1** for Power Supply Decoupling.

Table 1: Power Supply Pins Assignment of the CH7108B (QFN)

Pin Assignment	# Of Pins	Type	Symbol	Description
1	1	Power	VDDPLL	PLL Power Supply (1.2V)
2, 18	2	Power	DVDD	Digital supply voltage (1.2V)
3, 19	2	GND	DGND	Digital Ground
11, 38	2	Power	AVCC	Analog supply voltage (3.3V)
24, 27	2	Power	AVCC_DAC	DAC power supply (2.5V~3.3V)
35	1	Power	AVDD	HDMI receiver power supply (1.2V)
Thermal pad	1	Ground	GND	Power supply ground

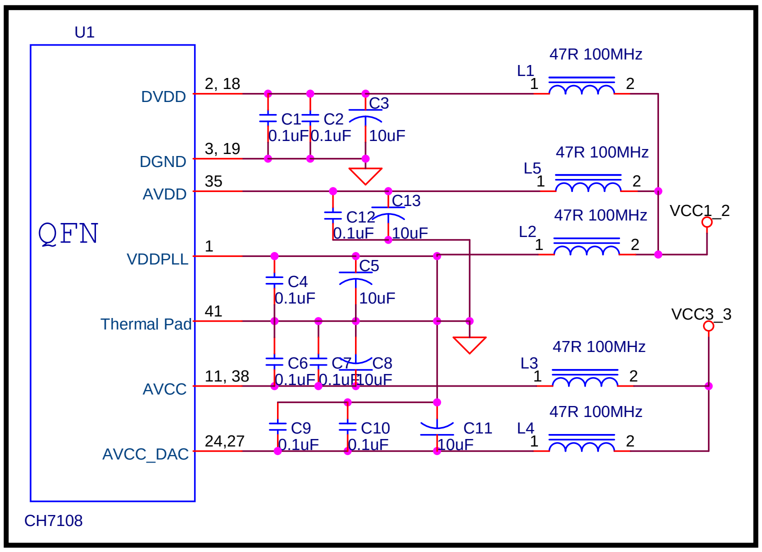


Figure 1: Power Supply Decoupling and Distribution

Note: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05 Ω at DC; 23 Ω at 25MHz & 47 Ω at 100MHz. Please refer to Fair Rite part #2743019447 for details or an equivalent part can be used for the diagram.

2.2 Internal Reference Pins

• RBIAS pin

This pin sets the DAC current. A 10 KΩ, 1% tolerance resistor should be connected between RBIAS and GND as shown in **Figure 2**. A smaller resistance will create more DAC current. This resistor should be placed with short and wide traces as near as possible to CH7108B.

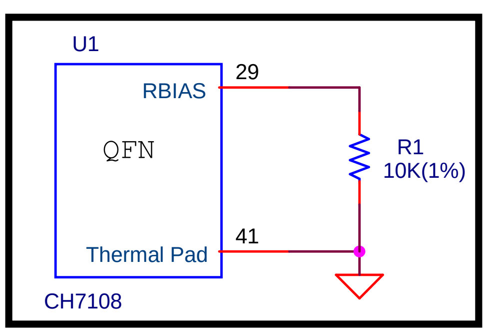


Figure 2: RBIAS pin connection

2.3 General Control Pins

• RB

This pin is the chip reset pin for CH7108B, which is internally pulled-up, places the device in the power on reset condition when this pin is low. A power-reset switch can be placed on the RB pin on the PCB as a hardware reset for CH7108B as shown in **Figure 3**. When the pin is high, the reset function can also be controlled through the serial port.

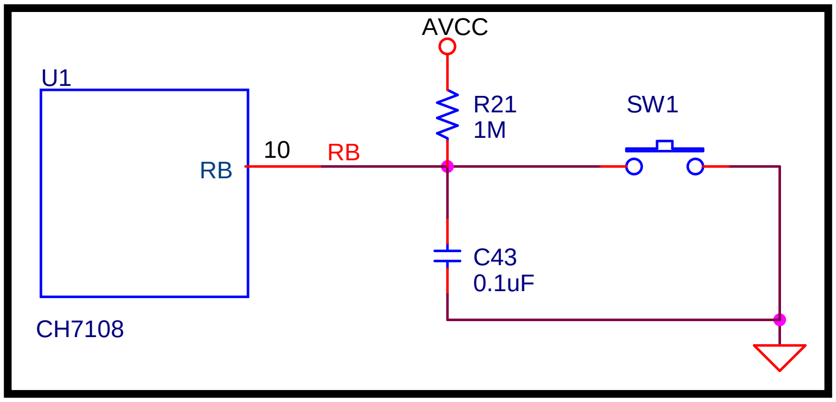


Figure 3: RB pin connection

• GPIO [1:0]

These pins are general-purpose input/output.

GPIO [1~0]=00 use crystal; GPIO [1~0]=01 not use crystal; GPIO [1~0]=10 not use crystal, only for 480P@60Hz

• XI/FIN and XO

CH7108B have capability to accept external crystal with frequencies 27 MHz. The crystal must be placed as close as possible to the XI and XO pins, with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7108B, it is very important that noise should not couple into these input pins. Traces with fast edge rates should not be routed under or adjacent these pins. In addition, the ground reference of the external capacitors connected to the crystal pins must be connected very close to the CH7108B.

The crystal load capacitance, C_L, is usually specified in the crystal spec from the vendor. As an example to show the load capacitors **Figure 4** gives a reference design for crystal circuit design.

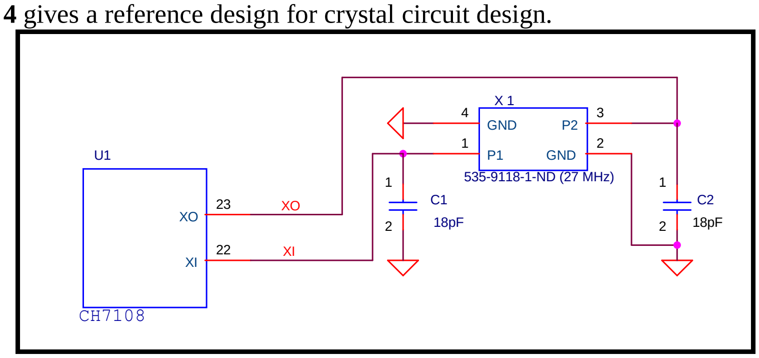


Figure 4: XI, XO pin connection

• Reference Crystal Oscillator

CH7108B integrate an oscillator circuit that allows a predefined-frequency crystal to be connected directly. Alternatively, an externally generated clock source may be supplied to CH7108B. If an external clock source is used, it should be of CMOS level specifications. The clock should be connected to the XI pin, and the XO pin should be left open. The external source must exhibit ±20ppm or better frequency accuracy, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be predefined-frequency, ±20 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to CH7108B (C_{ext}).

To be able to tune, a variable capacitor may be connected from XI to ground.

Note that the XI and XO pins each has approximately 10 PF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI and XO pins, the following calculation should be used:

$\mathbf{C}_{ext} = (2 \times C_L) - C_{int} - 2C_S$

Where
C_{ext} = external load capacitance required on XI and XO pins.

C_L = crystal load capacitance specified by crystal manufacturer.

C_{int} = capacitance internal to CH7108B (approximately 10-15 pF on each of XI and XO pins).

C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

In general,
$C_{int}XI = C_{int}XO = C_{int}$
$C_{ext}XI = C_{ext}XO = C_{ext}$

Such that
$C_L = (C_{int} + C_{ext}) / 2 + C_S$ and $C_{ext} = 2\,(C_L - C_S) - C_{int} = 2C_L - (2C_S + C_{int})$

Therefore C_L must be specified greater than $C_{int} /2 + C_S$ in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For detail considerations of crystal oscillator design, please refer to **AN-06**.

2.4 Serial Port Control for CH7108B

• SPC0 and SPD0

SPD0 and SPC0 function as a serial interface where SPD0 is bi-directional data and SPC0 is an input only serial clock. In the reference design, SPD0 and SPC0 pins are pulled up to +3.3V with 6.8K resistors always as shown in **Figure 5**.

• DDC_SCL and DDC_SDA

DDC_SCL and DDC_SDA are used to interface with the DDC of HDMI Source or transmitter and the serial PROM. This DDC pair needs to be pulled up to 5V through 47 KΩ resistors (Refer to **Figure 5**).

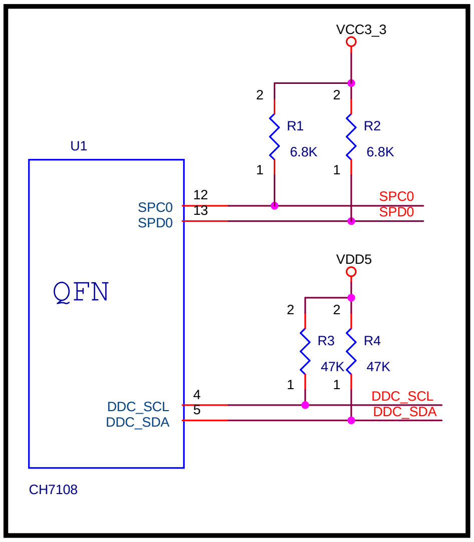


Figure 5: Serial Port Control

2.5 HDMI receiver Pins

The RCP, RCN, RD [2:0] P, RD [2:0] N signals are high frequency differential signals that need to be routed with special precautions. Since those signals are differential, they must be routed in pairs.

2.5.1 Differential Pair Impedance

To match the external cable impedance and maintain the maximal energy efficiency it is important to meet the impedance target of 100-Ω ± 10% for the differential data/clock traces. The restriction of this impedance target is to prevent any loss of signal strengths resulting from a reflection of unwanted signals. The impedance can be acquired by proper design of trace length, trace width, signal layer thickness, board dielectric, etc. The HDMI differential pairs should be routed on the top layer directly to the HDMI connector pads if possible.

2.5.2 Trace Routing Length

To prevent from capacitive and impedance loading, trace lengths should be kept as minimal as possible. Vias and bends should always be minimized; inductive effects may be introduced, causing spikes in the signals. Trace routing lengths from CH7108B to the HDMI connector are limited to a maximum of 2 inches. The CH7108B should be as close to the HDMI connector as possible.

2.5.3 Length Matching for Differential Pairs

The HDMI specifies the intra-pair skew and the inter-pair skew as in **Table 2**. The intra-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between the true and complement signals. The inter-pair skew is the maximum allowable time difference on both low-to-high and high-to-low transitions between any two single-ended data signals that do not constitute a differential pair.

Table 2: Maximum Skews for the HDMI Transmitter

Skew Type	Maximum at Transmitter
Intra-Pair Skew	0.15 T_{bit}
Inter-Pair Skew	0.20 T_{Pixel}

Where T_{bit} is defined as the reciprocal of Data Transfer Rate and T_{Pixel} is defined as the reciprocal of Clock Rate. Therefore, T_{Pixel} is 10 times T_{bit}. In other words, the intra-pair length matching is much more stringent than the inter-pair length matching.

It is recommended that length matching of both signals of a differential pair be within 5 mils. Length matching should occur on a segment-by-segment basis. Segments might include the path between vias, resistor pads, capacitor pads, a pin, an edge-finger pad, or any combinations of them, etc. Length matching from one pair to any other should be within 100 mils.

Note that lengths should only be counted to the pins or pad edge. Additional etch within the edge-finger pad, for instance, is electrically considered part of the pad itself.

2.5.4 ESD Protection for HDMI Interface

In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each HDMI input (data and clock).

International standard EN 55024:1998 establishes 4kV as the common immunity requirement for contact discharges in electronic systems. 8kV is also established as the common immunity requirement for air discharges in electronic systems. International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 establishes the immunity testing and measurement techniques.
System level ESD testing to International standard EN 61000-4-2:1995 / IEC 1000-4-2:1995 has confirmed that the proper implementation of Chrontel recommended diode protection circuitry, using BCD AT1140 diode array devices, will protect the CH7108B device from HDMI transmitter discharges of greater than 19kV (contact) and 20kV (air). The AT1140 have a typical capacitance of only 0.50pF between I/O pins. This low capacitance won't bring too much bad effect on HDMI eye diagram test.

Figure6 (A) and **(B)** show the connection of HDMI connectors, including the recommended design of AT1140 diode array devices. HDMI connector is used to connect the CH7108B HDMI inputs from HDMI transmitter.

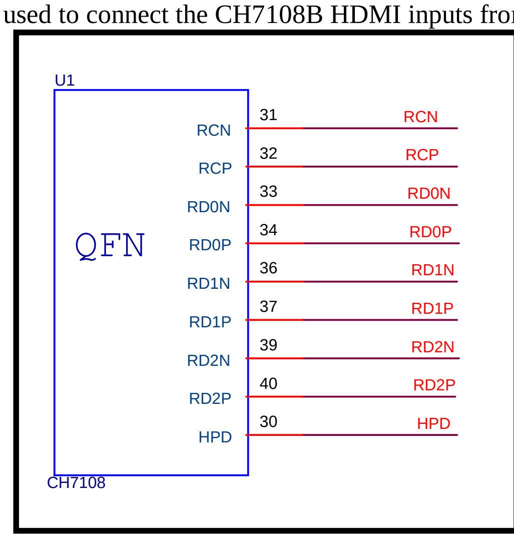


Figure 6(A): The connection of the HDMI input

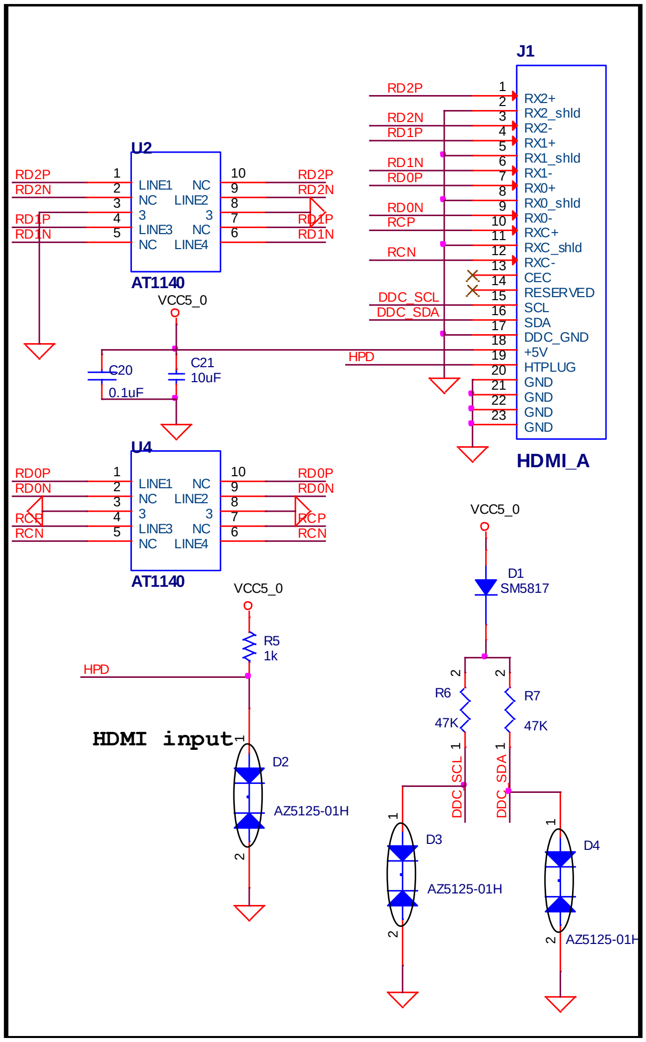


Figure 6(B): The connection of the HDMI inputs－CH7108B HDMI connectors

The following is the description for each HDMI interface pins

• HDMI Link Data Channel (RD [2:0] P and RD [2:0] N)

These pins provide HDMI differential inputs for data channel 0 (blue), data channel 1 (green) and data channel 2 (red). (Refer to **Figure 6 (A)**).

• HDMI Link Clock Outputs (RCP and RCN)

These pins provide the HDMI differential clock inputs for HDMI corresponding to data on the RD [2:0] P and RD [2:0] N inputs (Refer to **Figure 6 (A)**).

• HPD (HDMI Hot Plug Detect)

This output pin connects to the +5V power through a 1KΩ resistor. Refer to **Figure 6 (B)** for the design example.

2.6 SDTV Outputs

• CVBS (SDTV) output

Three on-chip 9-bit high speed DACs provide CVBS and S-Video (SDTV) output. If the DACs require a double termination, A 75 Ω resistor should be placed between each DAC pin and the ground as shown in **Figure 7.** (Refer to **Figure 7**)

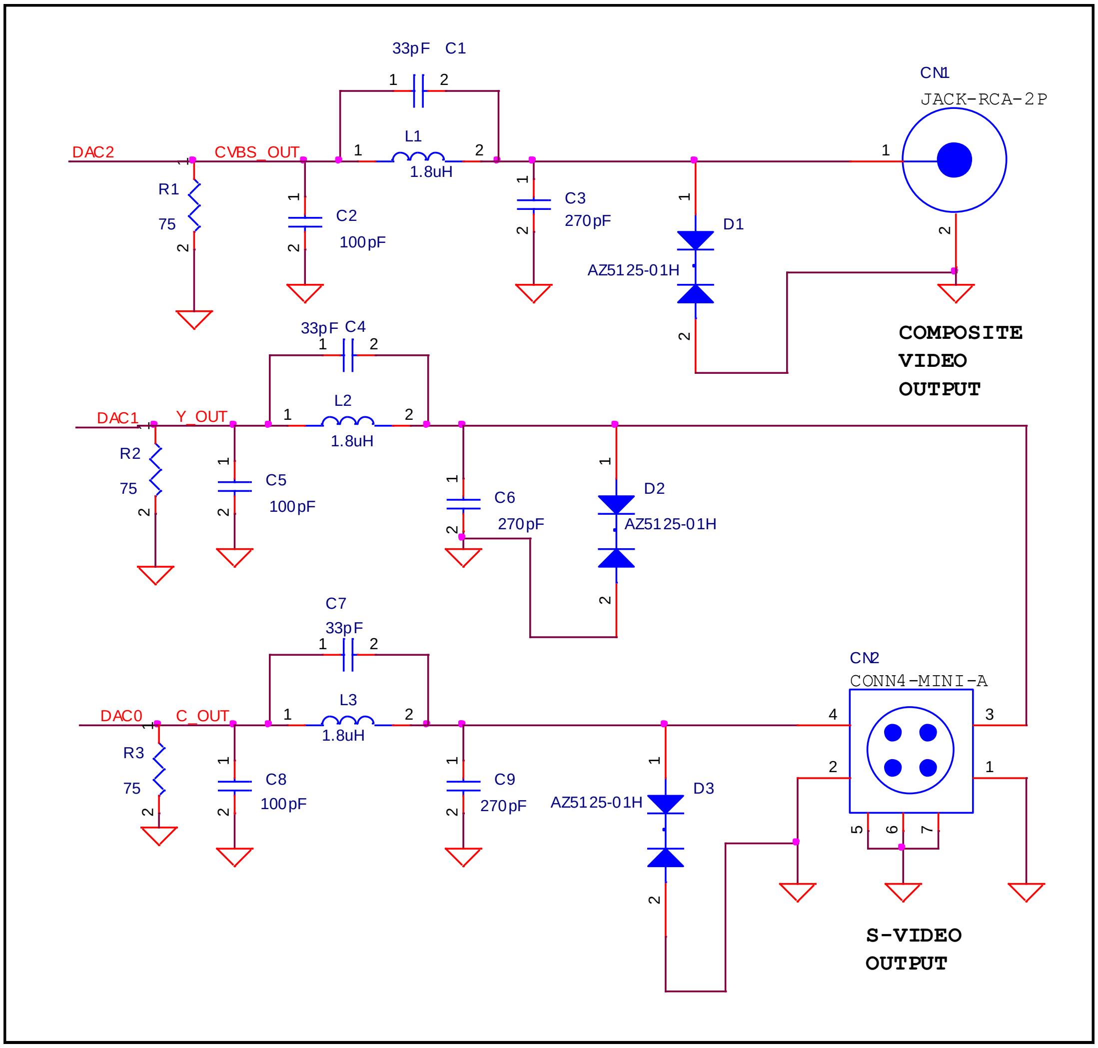


Figure 7: CH7108B CVBS and S-Video (SDTV) output

2.7 Audio Output

• IIS

IIS audio output can be configured through programming CH7108B registers. (Refer to **Figure 8**)

• SPDIF

For SPDIF output, CH7108B supports audio sample frequencies from 32Khz to 192kHz. (Refer to **Figure 8**)

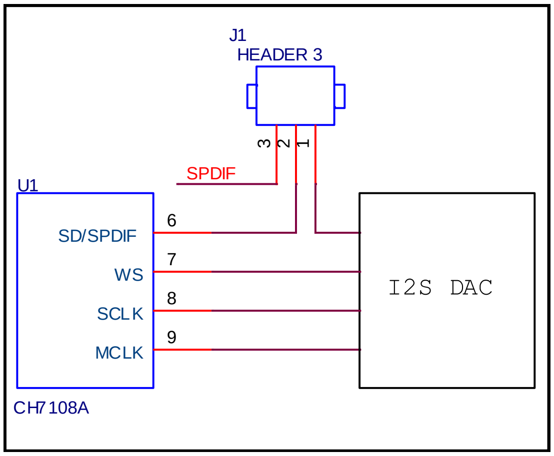
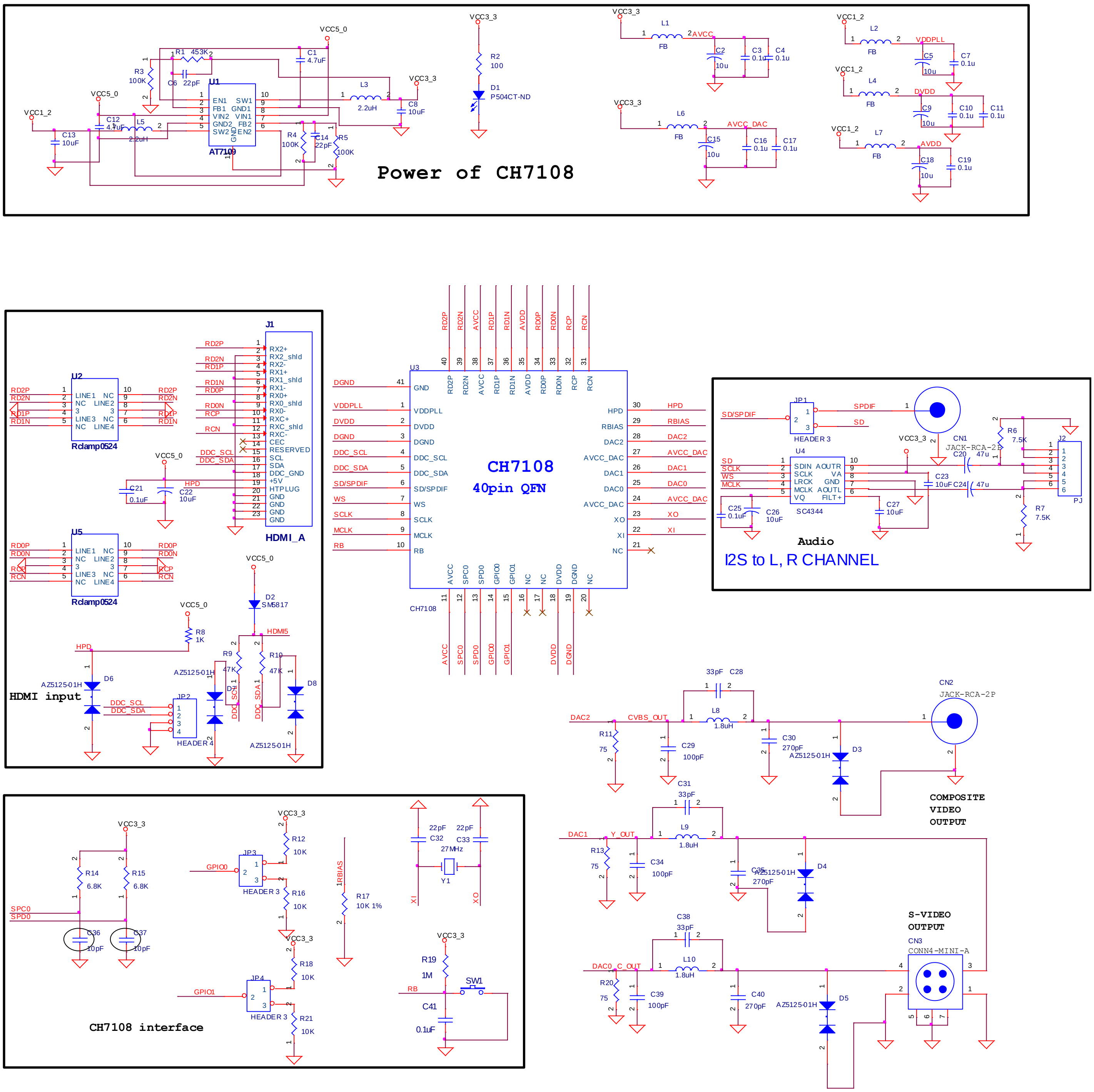


Figure 8: CH7108B IIS or SPDIF Output Pins

3.0 Reference Design Example

The figures below are the reference schematic of CH7108B, which is provided here for design reference only. Please contact Chrontel Applications group for further support. **Table 3** provides the BOM list for the reference schematic.

3.1 Reference Schematic



3.2 Reference Board Preliminary BOM

Table 3: CH7108B Reference Design BOM List

Item	Quantity	Reference	Part
1	2	CN1, CN2	RCA Jack
2	1	CN3	4-Mini DIN
3	2	C1, C12	4.7uF
4	4	C6, C14, C32, C33	22pF
5	11	C2, C5, C8, C9, C13, C15, C18, C22, C23, C26, C27	10uF
6	11	C3, C4, C7, C10, C11, C16, C17, C19, C21, C25, C41	0.1uF
7	3	C28, C31, C38	33pF
8	3	C29, C34, C39	100pF
9	3	C30, C35, C40	270pF
10	2	C20, C24	47uF
11	2	C36, C37	10pF
12	1	D2	SM5817
13	1	D1	P504CT-ND
14	6	D3, D4, D5, D6, D7, D8	AZ5125-01H
15	3	JP1, JP3, Jp4	HEADER 3
16	1	JP2	HEADER 4
17	1	J1	HDMI_A
18	1	J2	PJ
19	5	L1, L2, L4, L6, L7	FB
20	2	L3, L5	2.2uH
21	3	L8, L9, L10	1.8uH
22	1	R1	453K 1%
23	1	R2	100
24	3	R5, R3, R4	100K 1%
25	1	R8	1k
26	2	R6, R7	7.5K
27	2	R9, R10	47K
28	3	R11, R13 R20	75
29	4	R12, R16, R18, R21	10K
30	2	R14, R15	6.8K
31	1	R17	10K 1%
32	1	R19	1M
33	1	SW1	SW
34	1	U1	AT7109
35	2	U2, U5	AT1140
36	1	U3	CH7108B
37	1	U4	CS4344
38	1	Y1	27MHz

4.0 REVISION HISTORY

Table 4: Revisions

Rev. #	Date	Section	Description
0.1	08/16/2013	All	Initial release
0.2	07/16/2015	All	Update for CH7108B

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